

FIG. 1

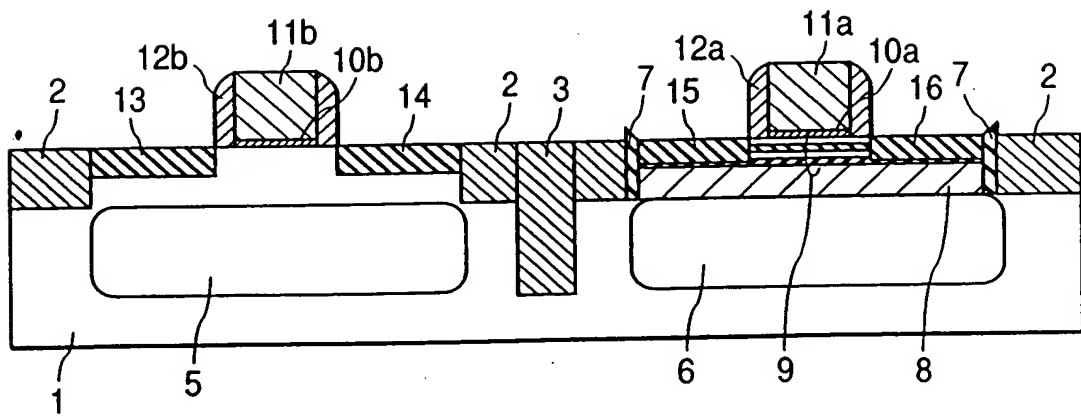


FIG. 2(a)

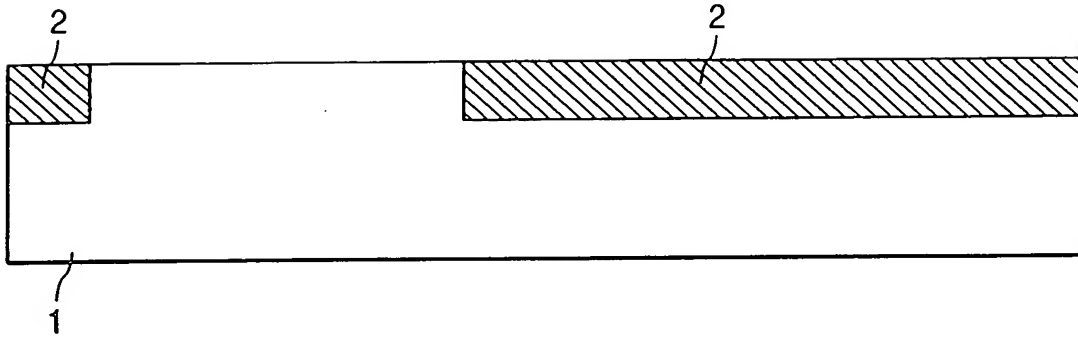


FIG. 2(b)

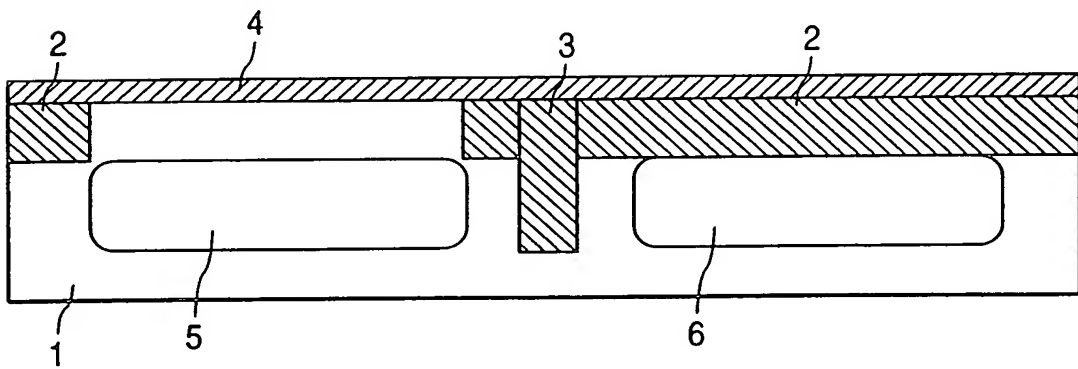


FIG. 2(c)

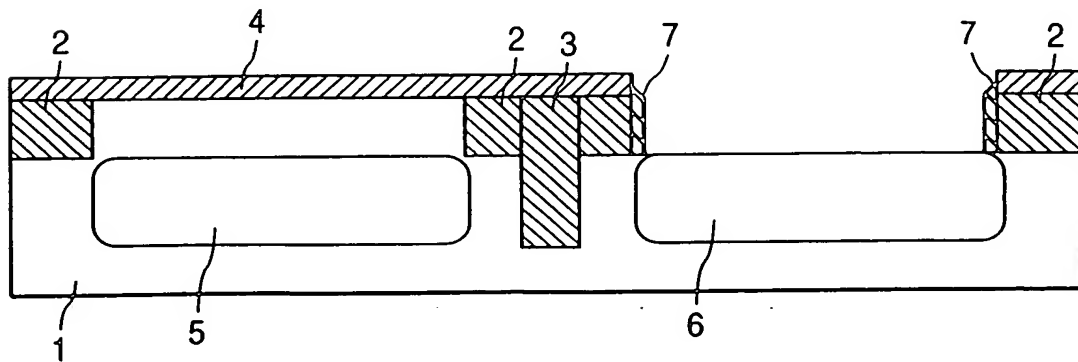


FIG. 3(a)

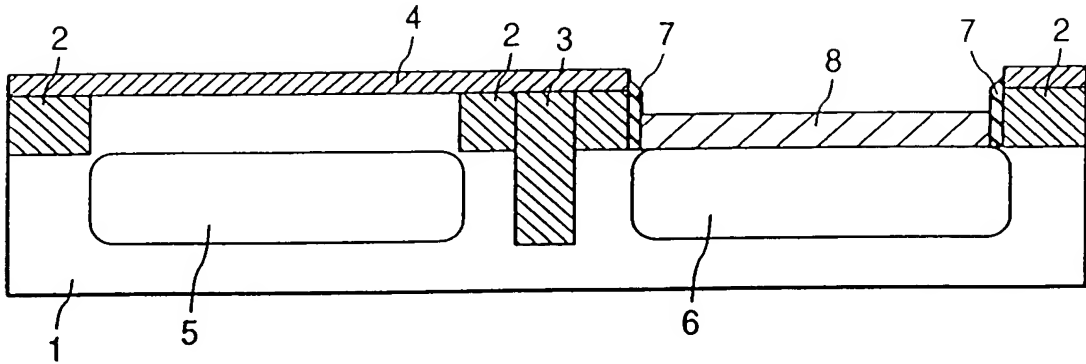


FIG. 3(b)

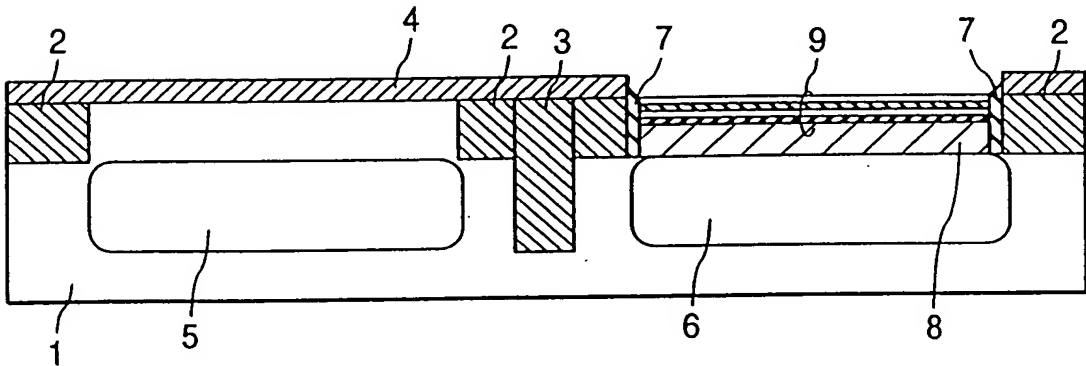


FIG. 3(c)

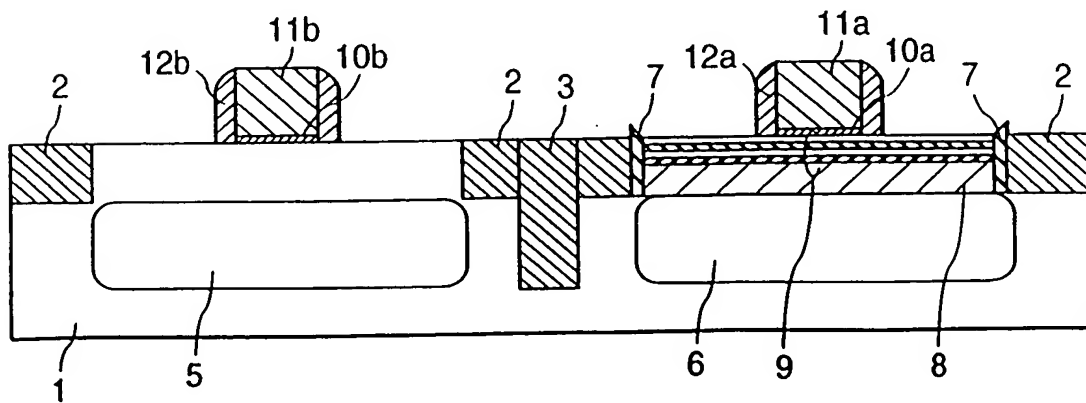


FIG. 4(a)

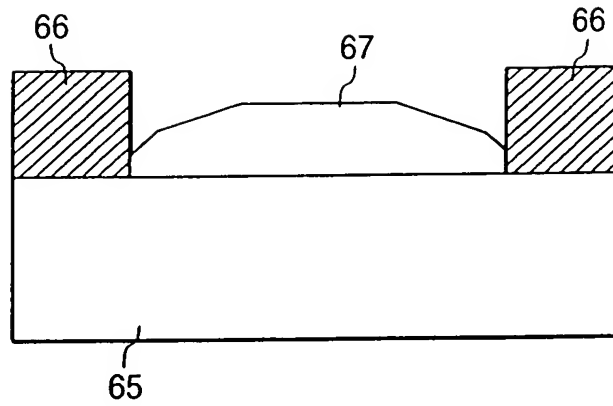


FIG. 4(b)

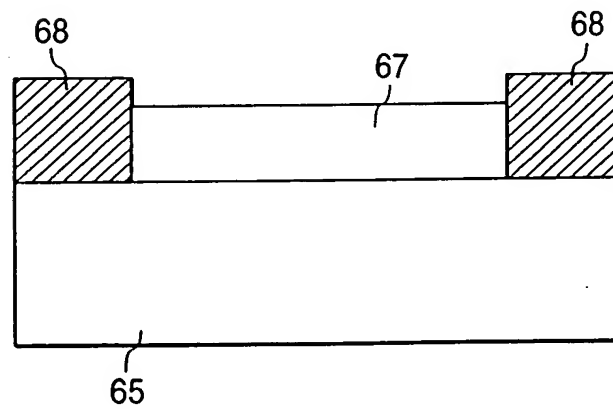


FIG. 5

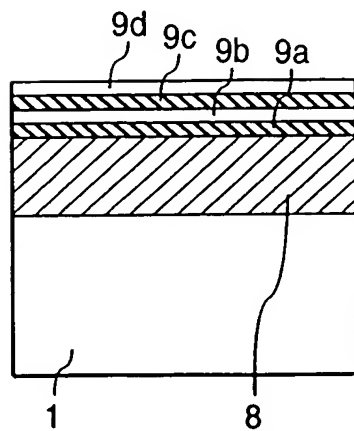


FIG. 6

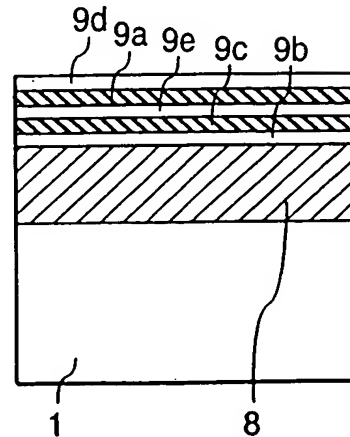


FIG. 7

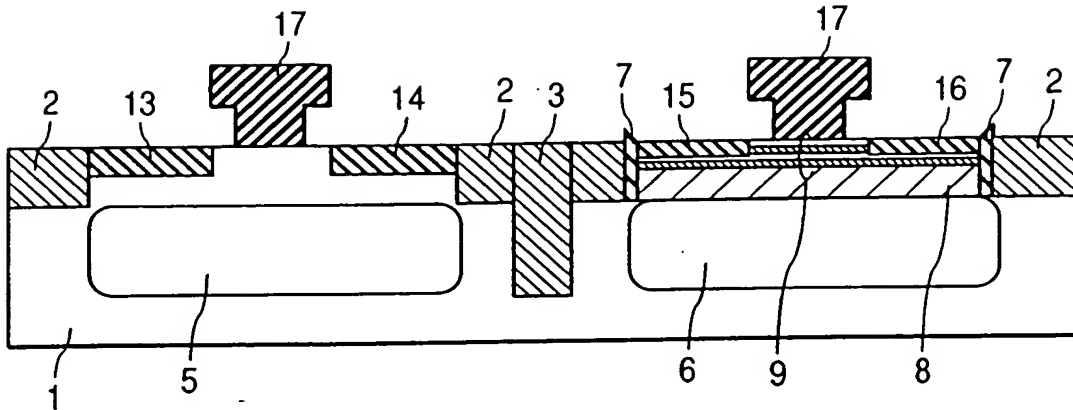


FIG. 8

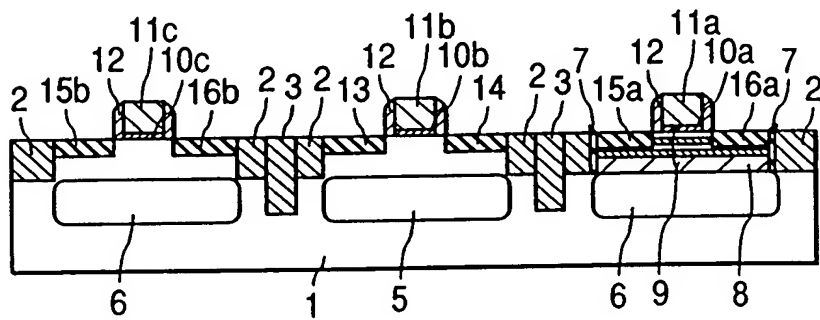


FIG. 9

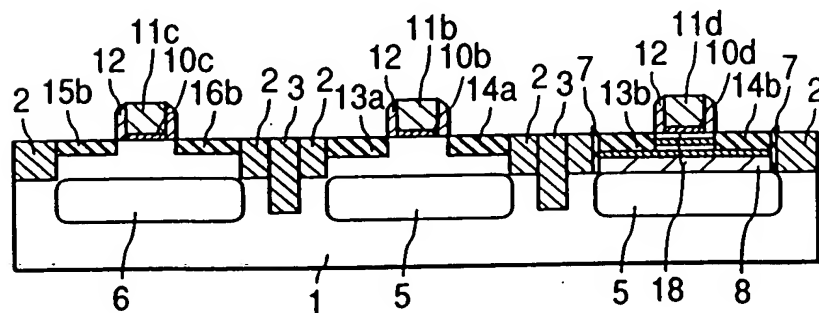


FIG. 10

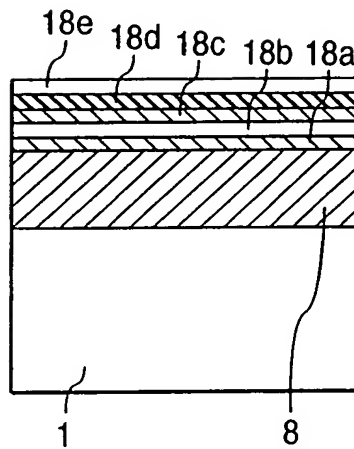


FIG. 11

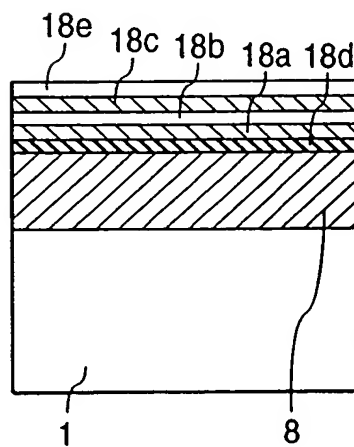


FIG. 12

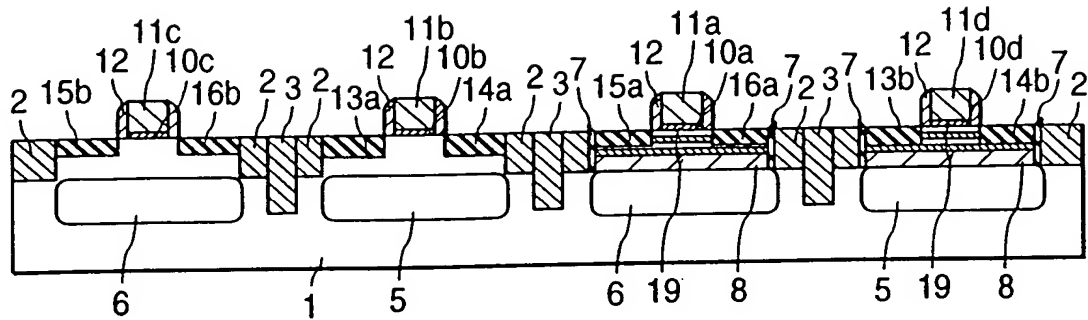


FIG. 13

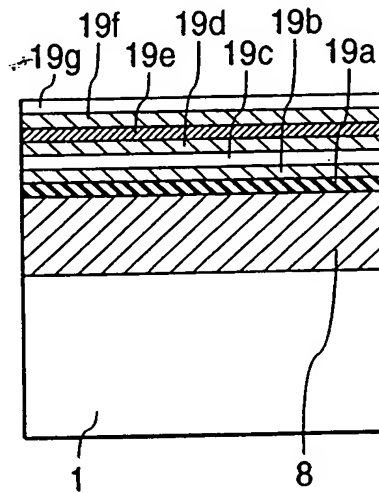


FIG. 14

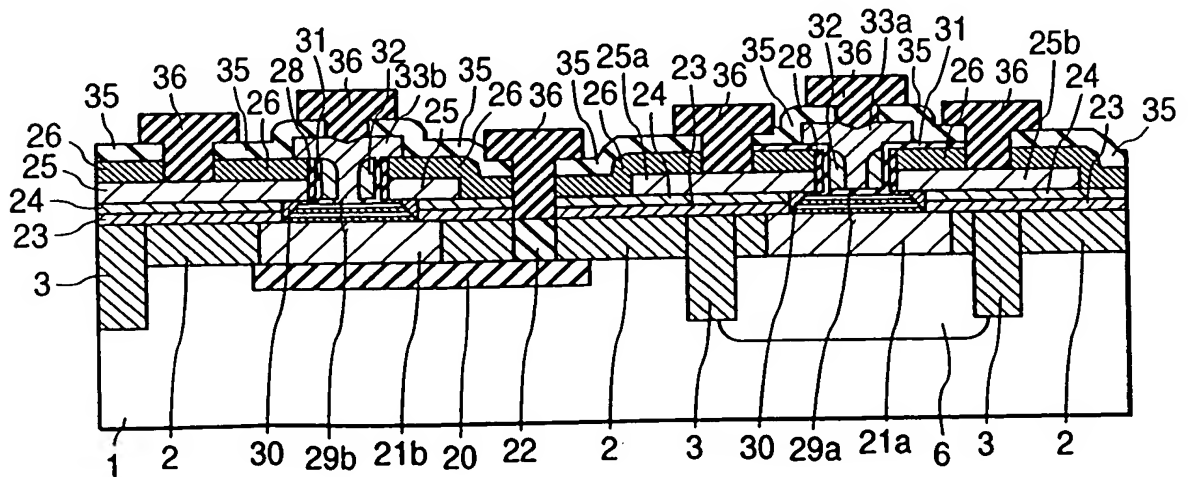


FIG. 15(a)

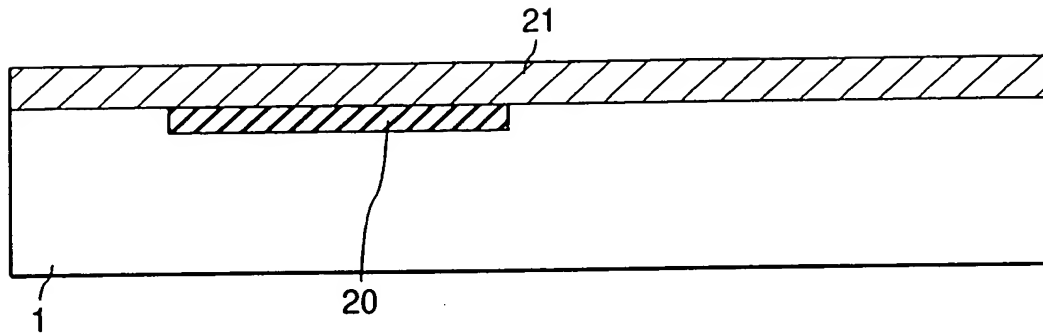


FIG. 15(b)

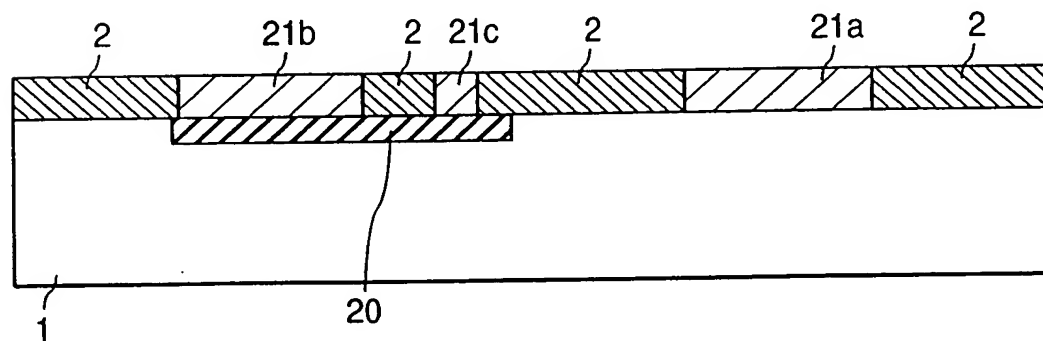
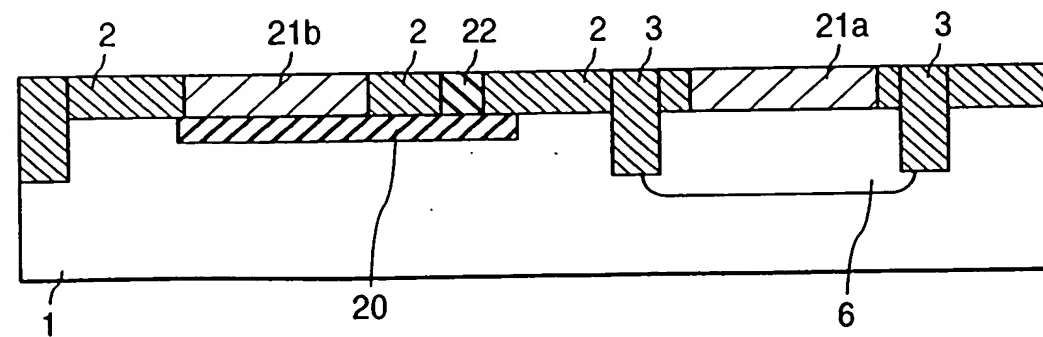


FIG. 15(c)



This diagram shows a cross-sectional view of a semiconductor device with two gate structures. The substrate is labeled 1. The first gate structure on the left includes a gate stack 24 on top of a gate 2, with a gate spacer 21b on the side. The second gate structure on the right includes a gate stack 24 on top of a gate 2, with a gate spacer 21a on the side. A central region 20 is located between the two gates, containing a structure 22. A layer 23 is positioned above the central region 20. A layer 25 is on top of the gate stacks 24. A layer 3 is on the side of the gates. A layer 6 is on the side of the central region 20.

This cross-sectional view shows a semiconductor device with a substrate (1) and a base layer (2). The device features a series of stacked layers and regions. From left to right, the layers are labeled 1, 2, 21b, 20, 22, 2, 3, 21a, 6, 3, and 2. The top layers are labeled 25c, 24, 23, and 26. The regions between the top layers are labeled 27 and 28. The device is shown in a cross-sectional view, with the layers and regions labeled 1 through 28.

This cross-sectional view shows a semiconductor device with a substrate (1) and a series of gate structures (26) separated by spacers (28). The gate structures are formed on a layer (24) over a layer (23). The substrate has regions labeled 1, 2, 30, 29b, 21b, 20, 22, 2, 3, 30, 29a, 21a, 6, 3, and 2. The gate structures are labeled 26, 28, 25c, 26, 25a, 24, 23, 28, 26, 25b, 24, 23. The device includes a layer (25c) and a layer (24) over a layer (23).

FIG. 18

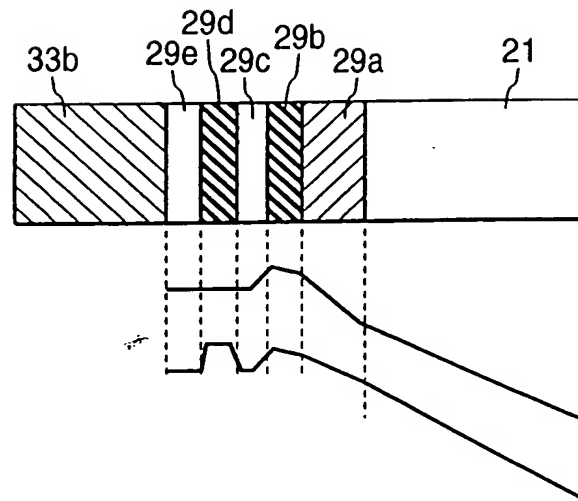


FIG. 19

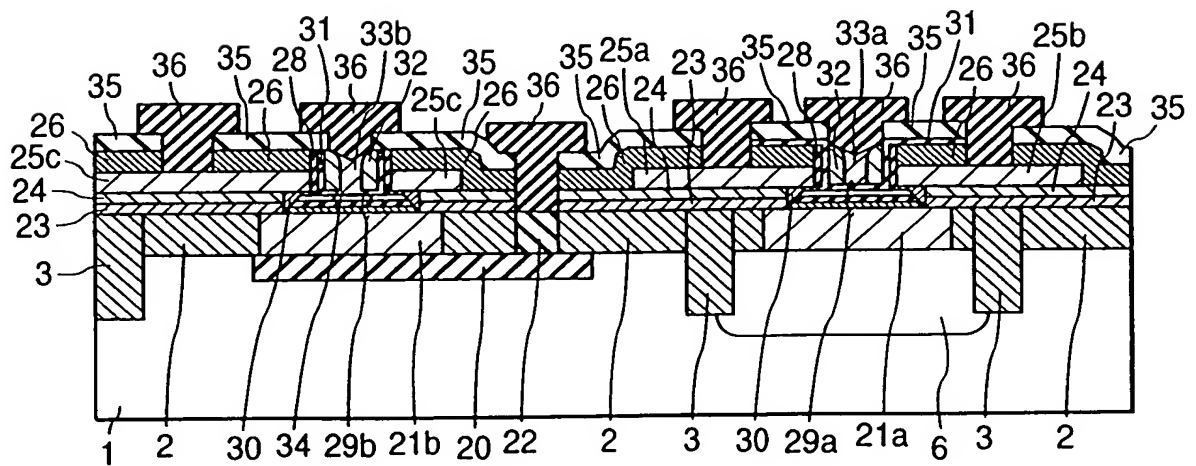


FIG. 20

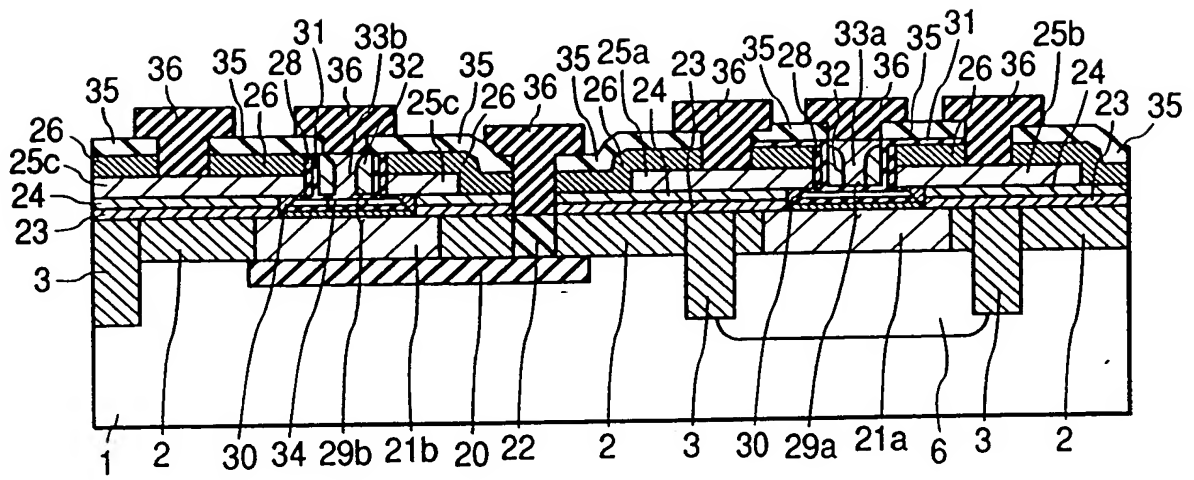


FIG. 21

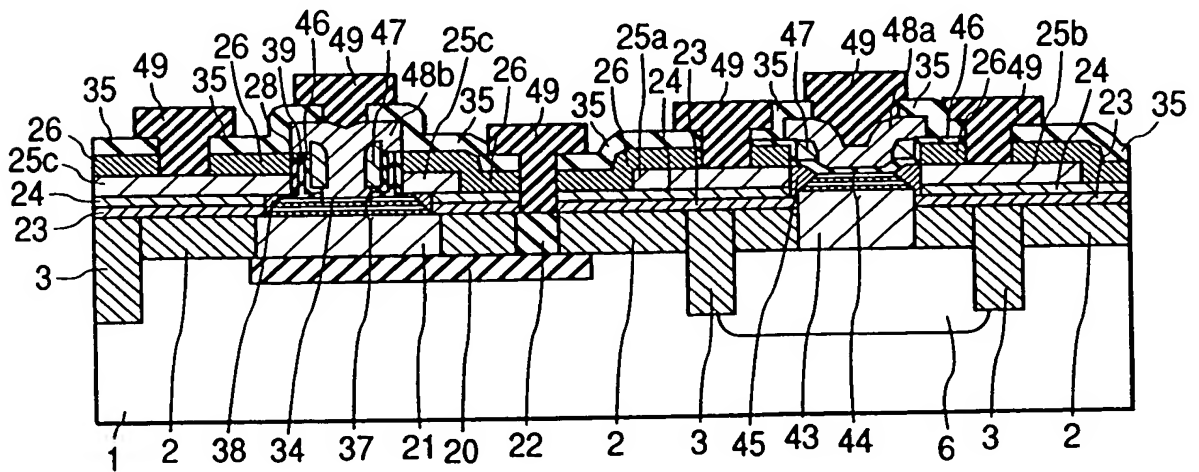


FIG. 22(a)

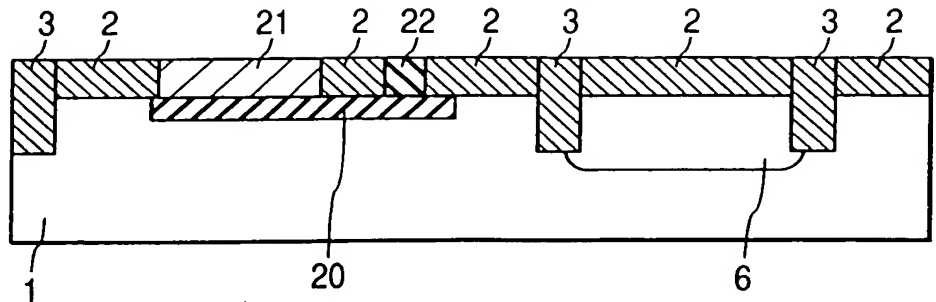


FIG. 22(b)

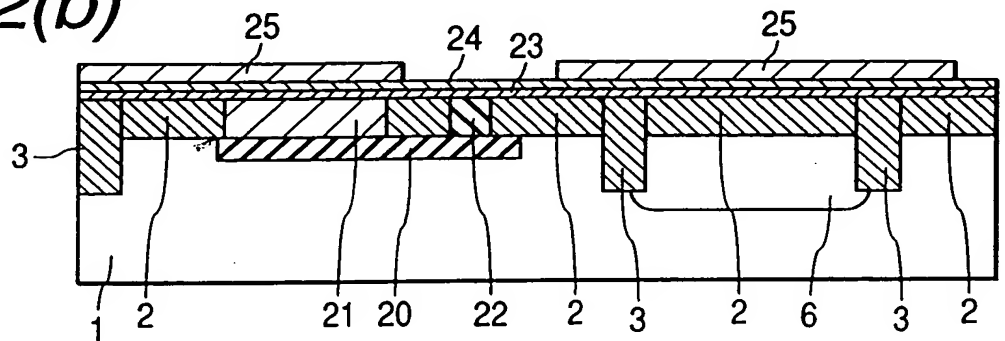


FIG. 22(c)

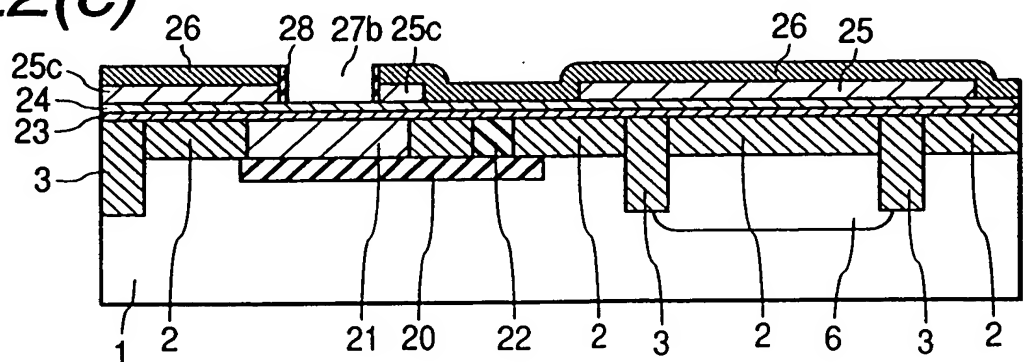


FIG. 22(d)

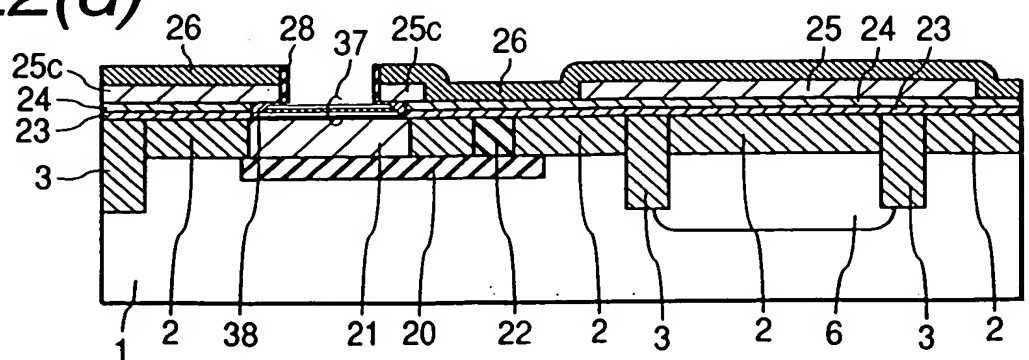


FIG. 23(a)

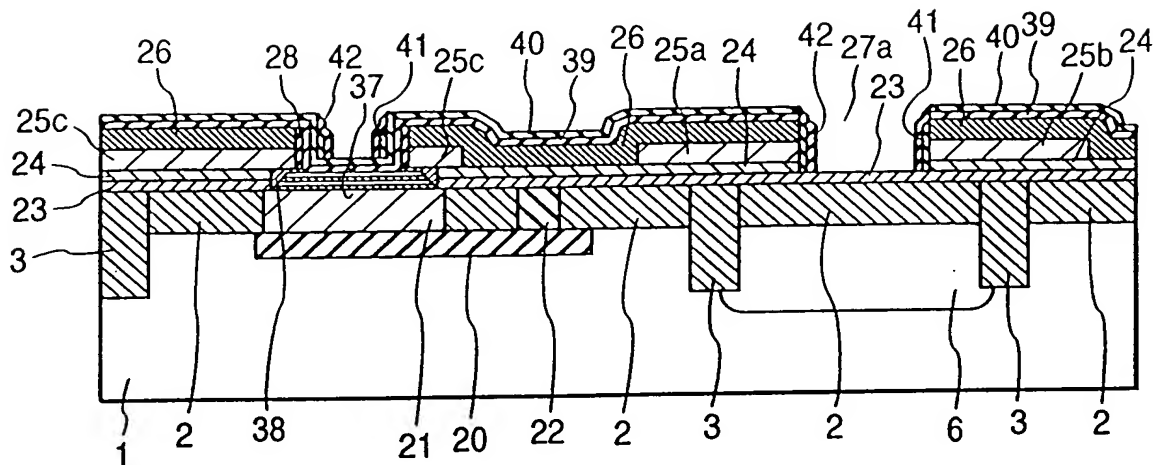


FIG. 23(b)

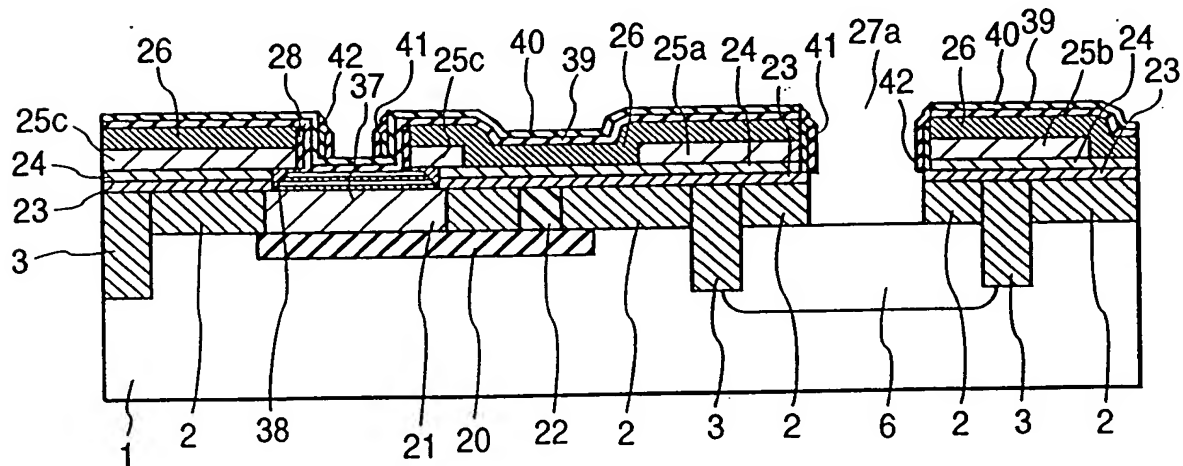


FIG. 23(c)

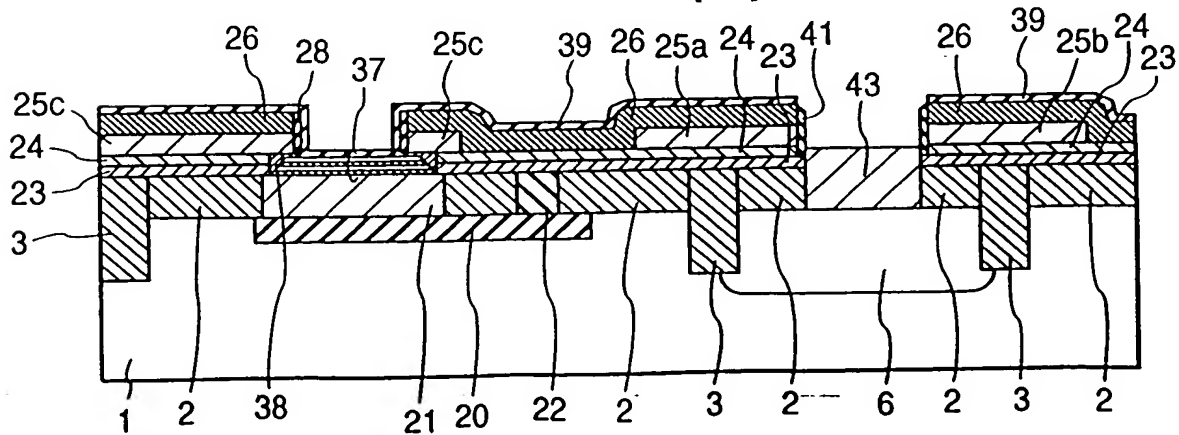


FIG. 25

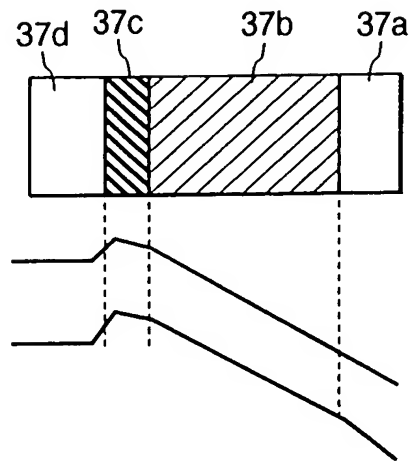


FIG. 26(a)

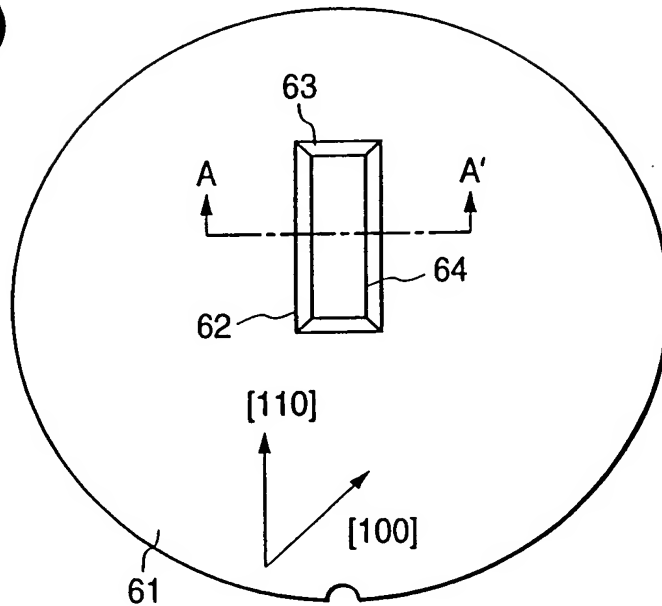


FIG. 26(b)

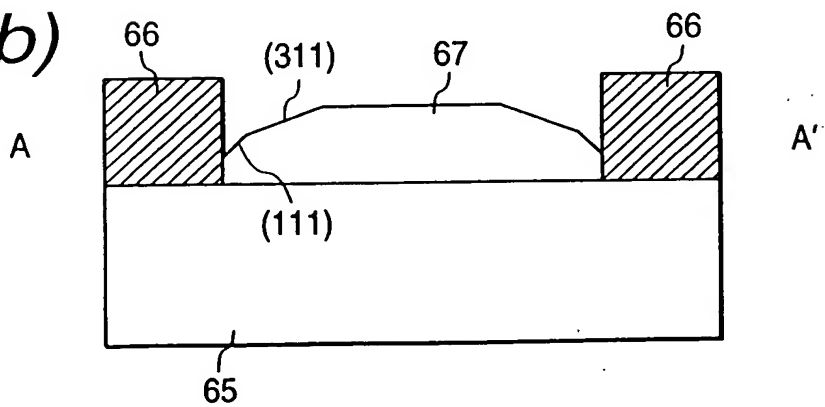


FIG. 27(a)

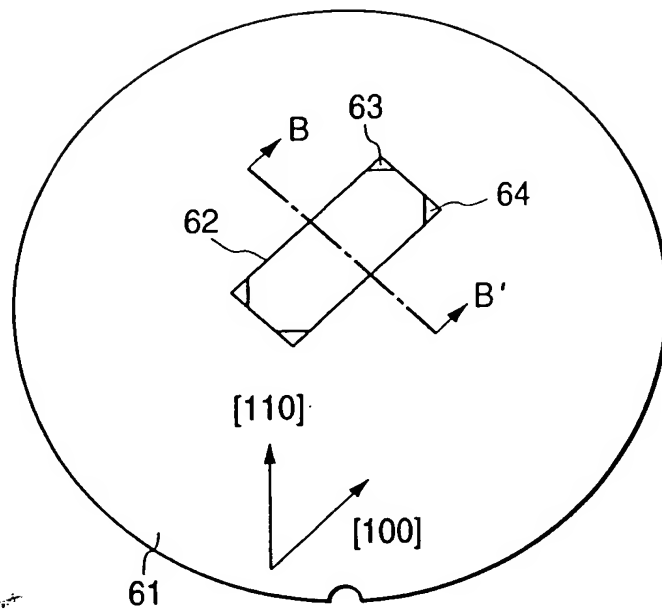


FIG. 27(b)

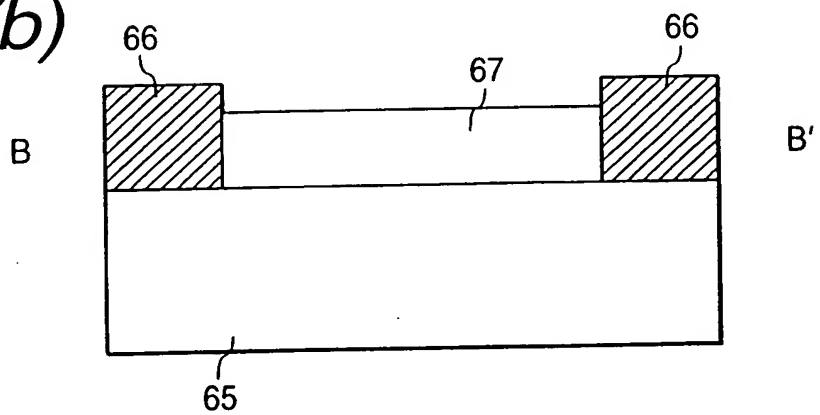


FIG. 28

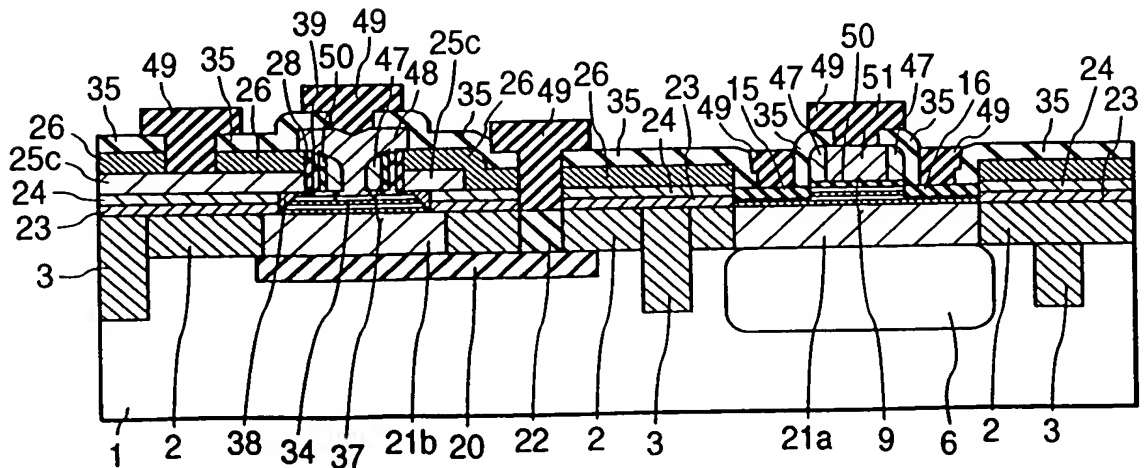


FIG. 29(a)

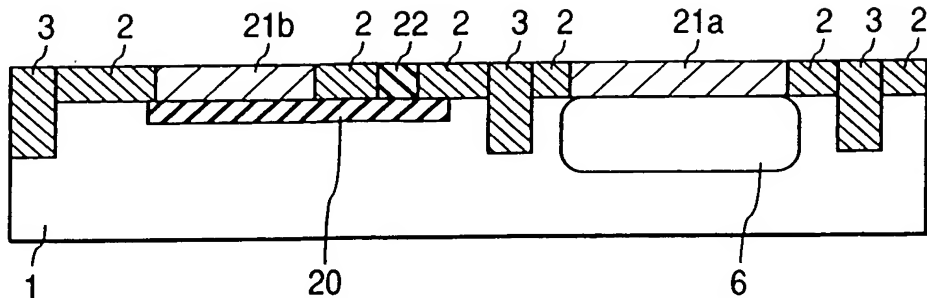


FIG. 29(b)

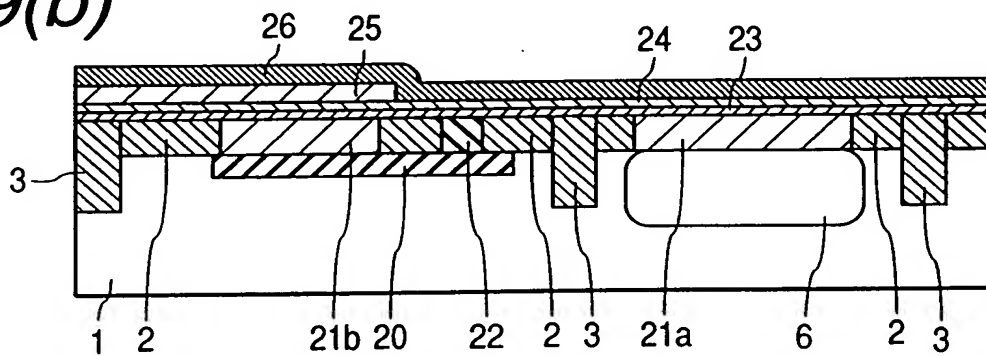


FIG. 29(c)

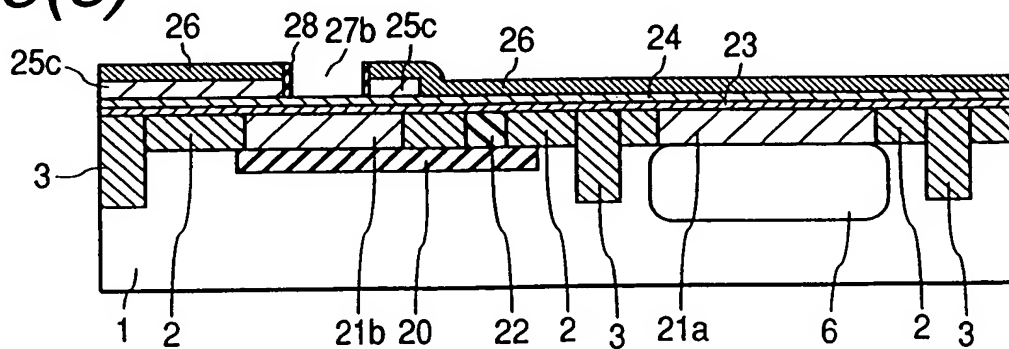
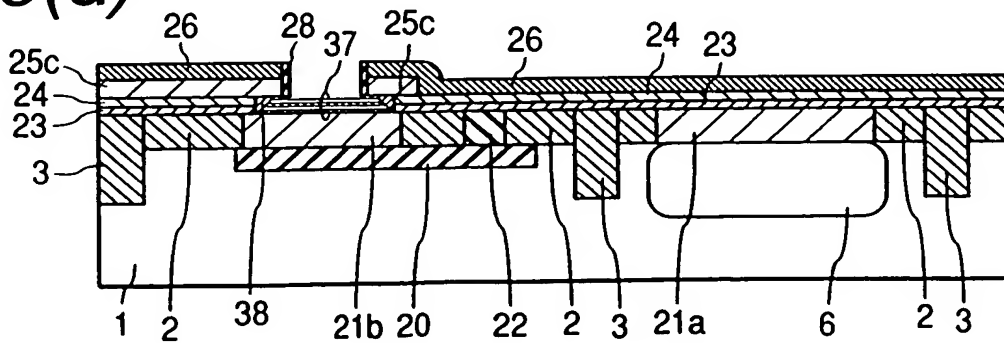


FIG. 29(d)



A detailed cross-sectional view of a multi-layered structure, likely a semiconductor device or a specialized electronic component. The structure consists of several horizontal layers and vertical features. Key components are labeled with numbers and letters: 1, 2, 3, 6, 9, 20, 21a, 21b, 22, 23, 24, 25c, 26, 28, 37, 38, 39, 47, 50, and 51. The layers are shown with different hatching patterns to distinguish them. A central horizontal layer (24) is prominent, with various structures built upon it. A large, rounded rectangular feature (21a) is located in the lower right portion of the structure. The overall design suggests a complex, multi-layered assembly.

[illegible]

FIG. 31

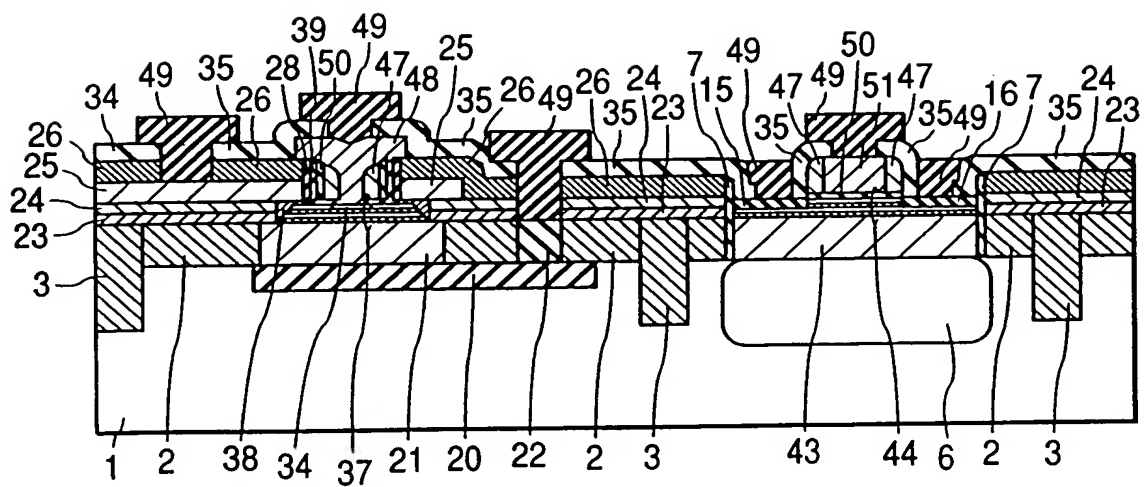


FIG. 32(a)

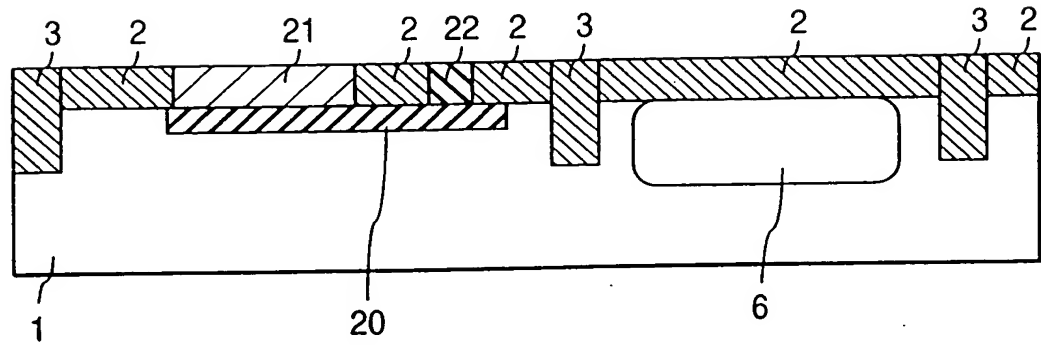


FIG. 32(b)

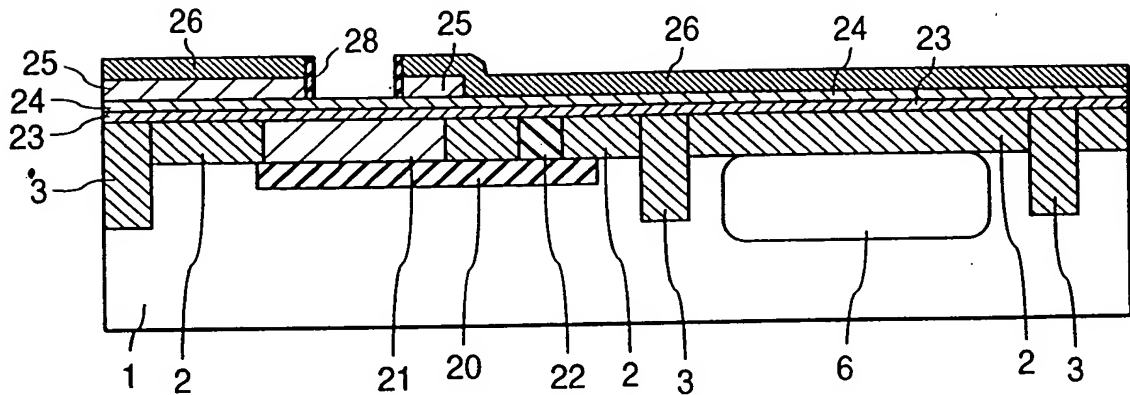


FIG. 32(c)

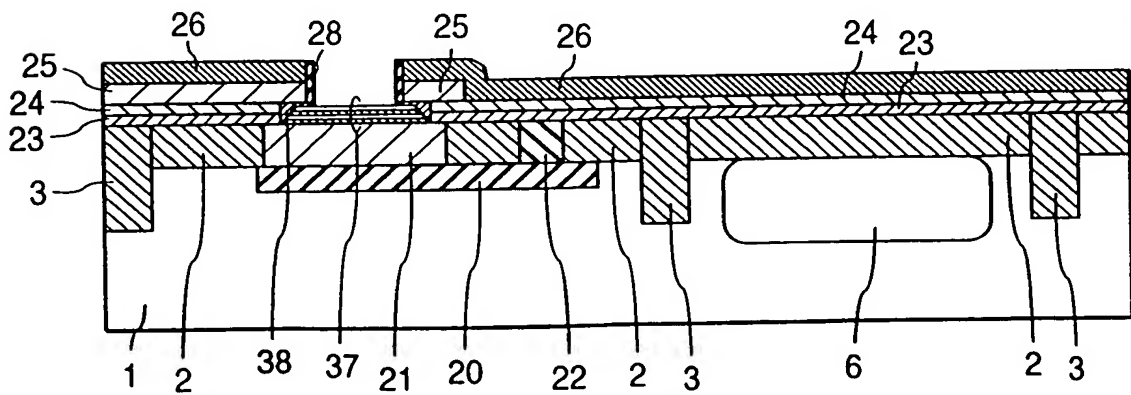


FIG. 33(a)

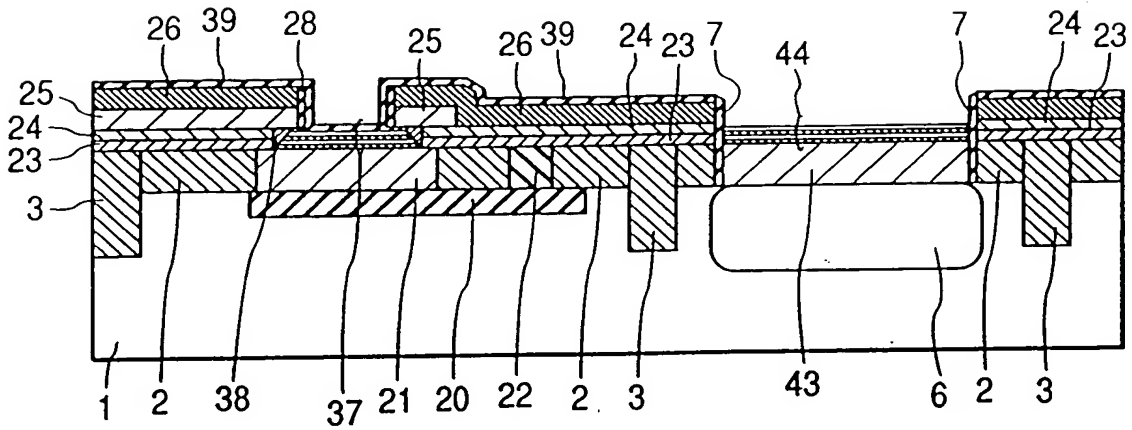


FIG. 33(b)

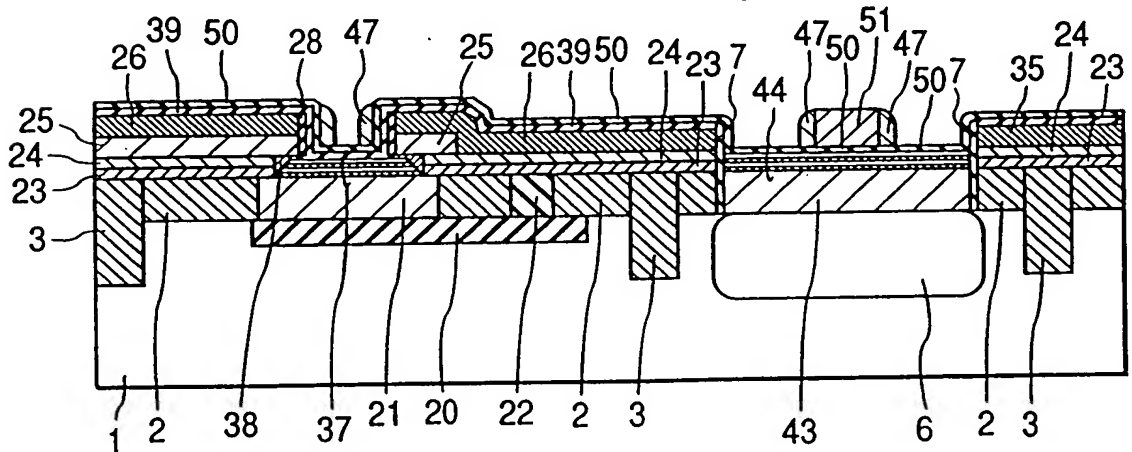


FIG. 33(c)

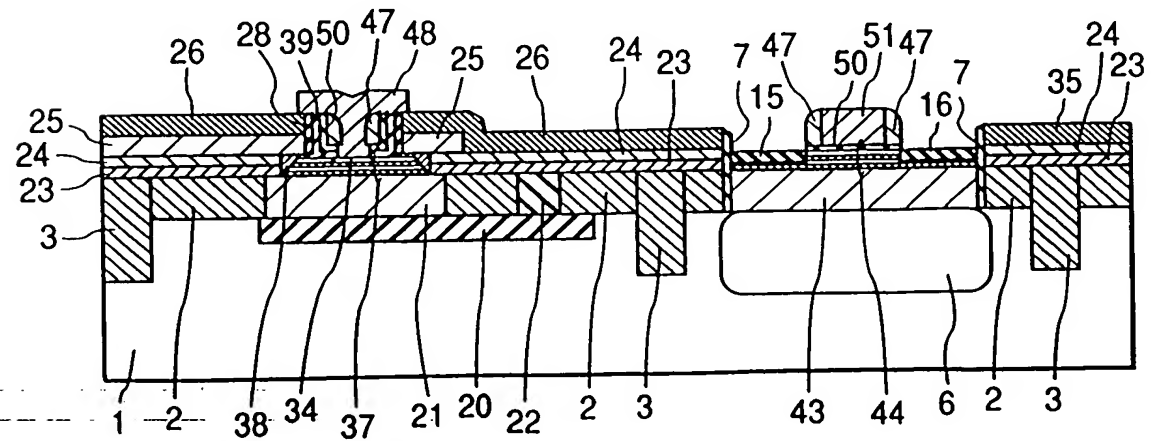


FIG. 36

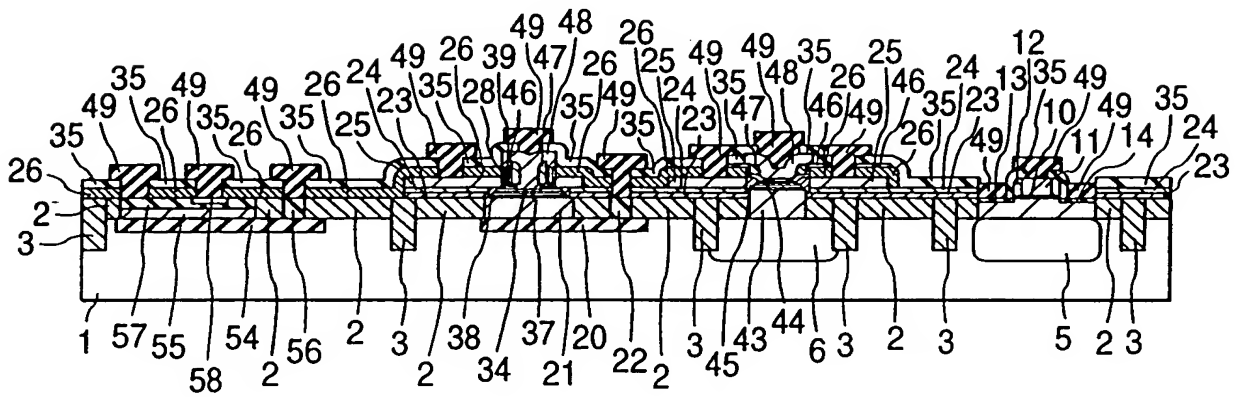


FIG. 37

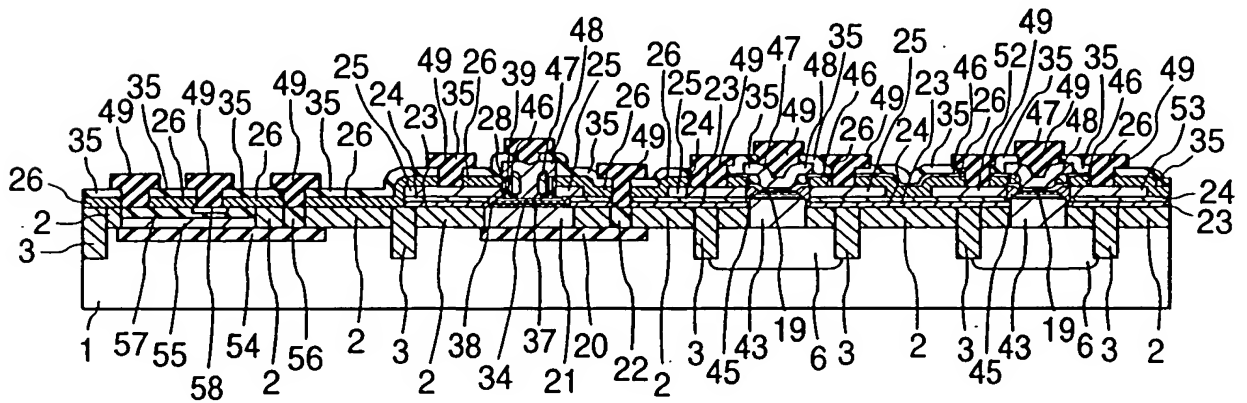


FIG. 38(a)

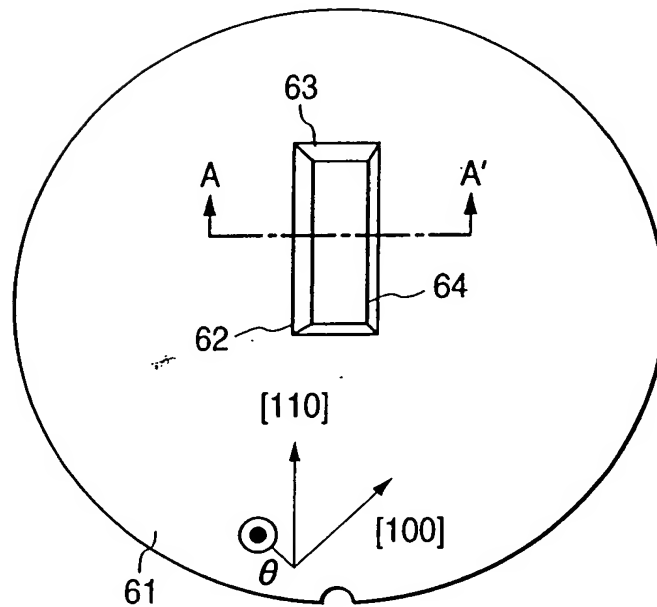


FIG. 38(b)

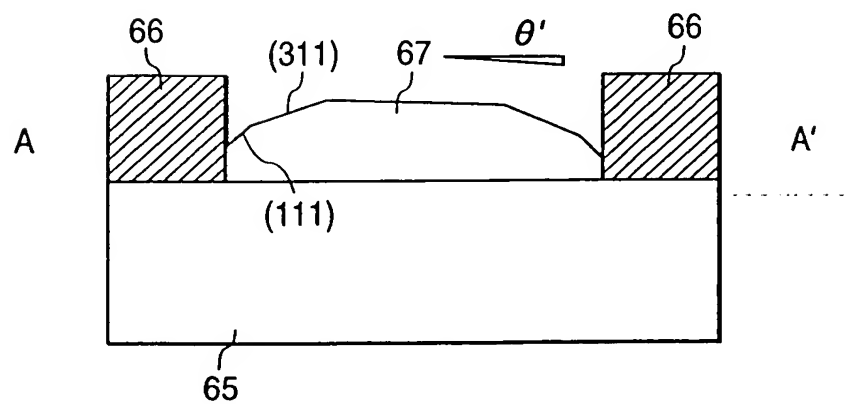


FIG. 39(a)

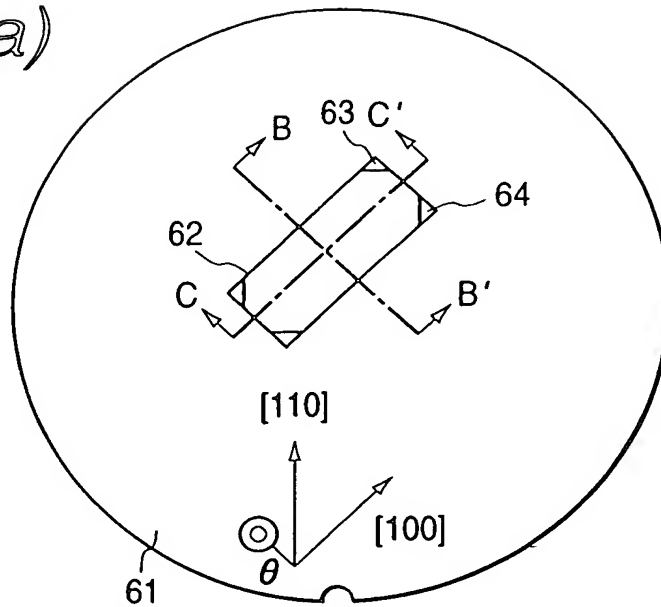


FIG. 39(b)

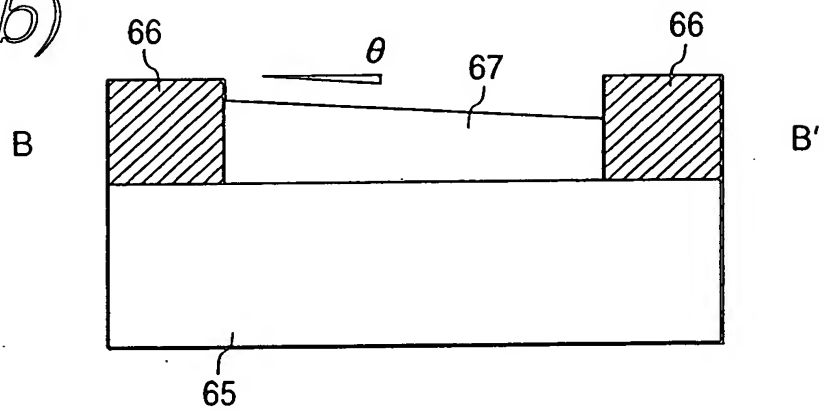


FIG. 39(c)

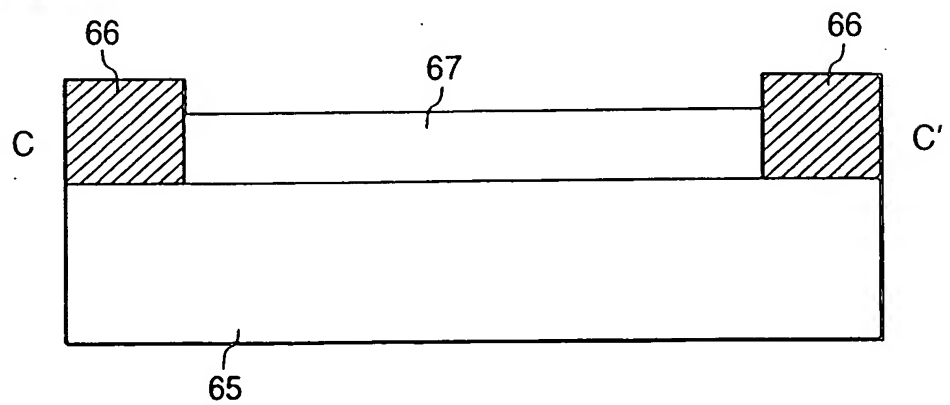


FIG. 40

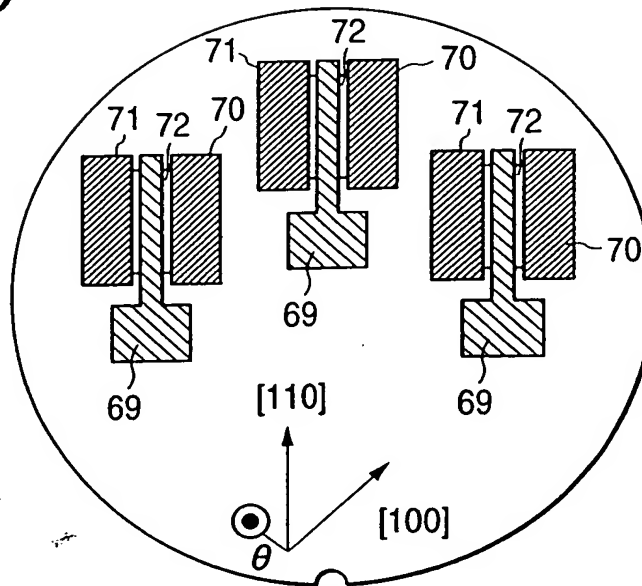


FIG. 41

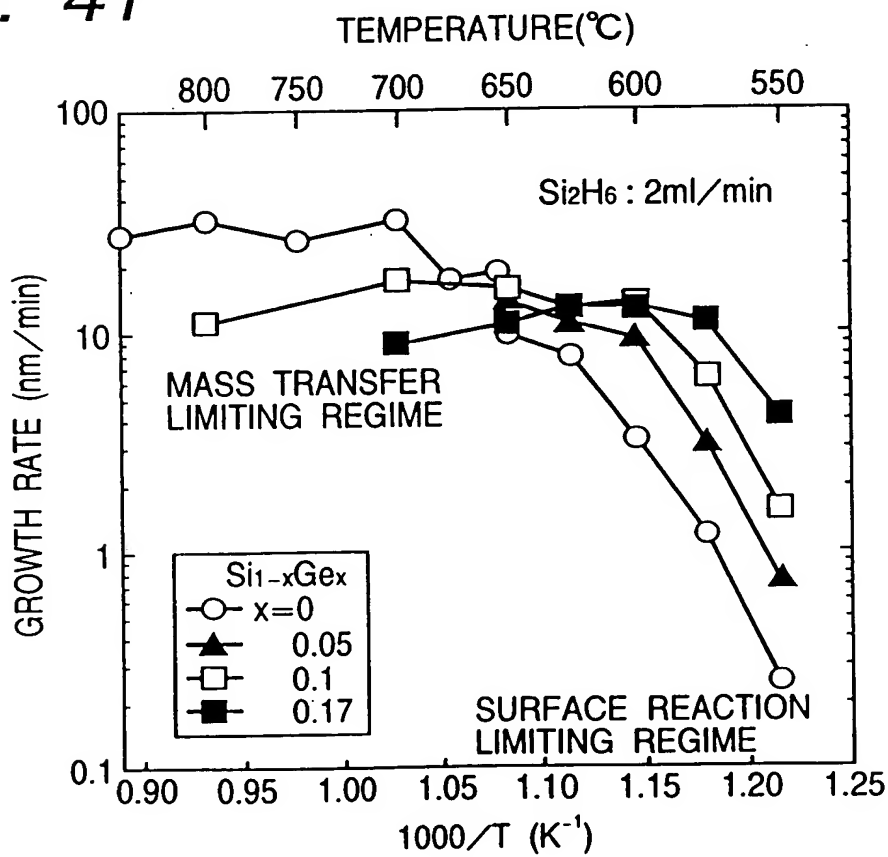


FIG. 42

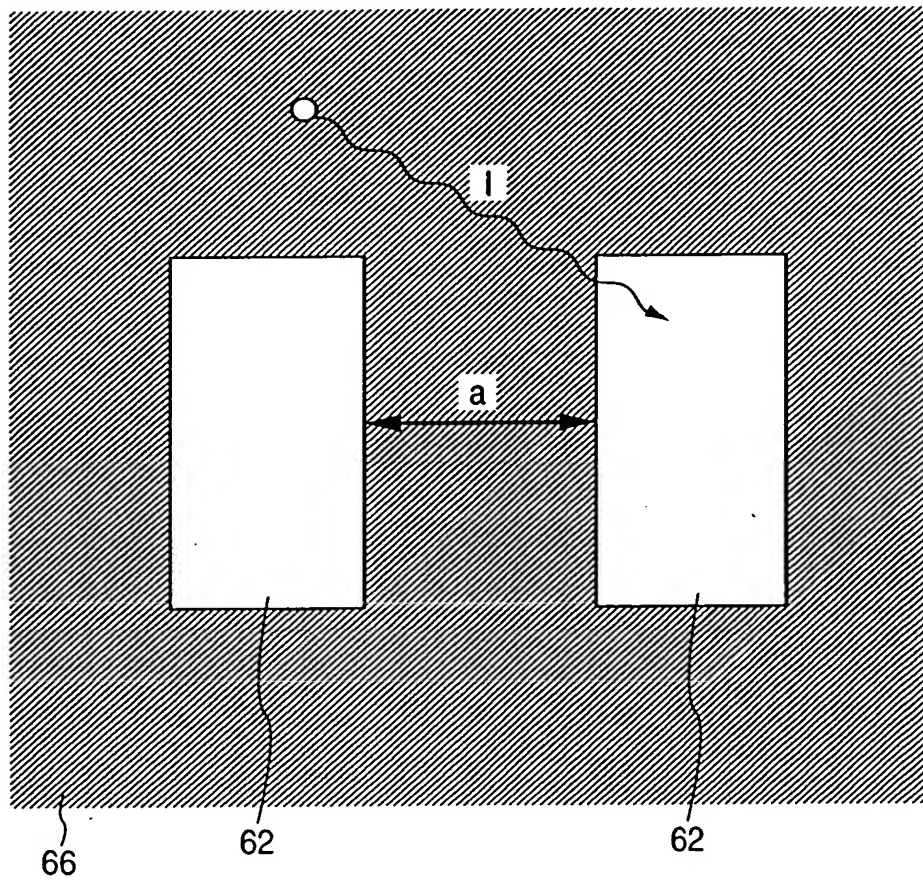


FIG. 43(a)

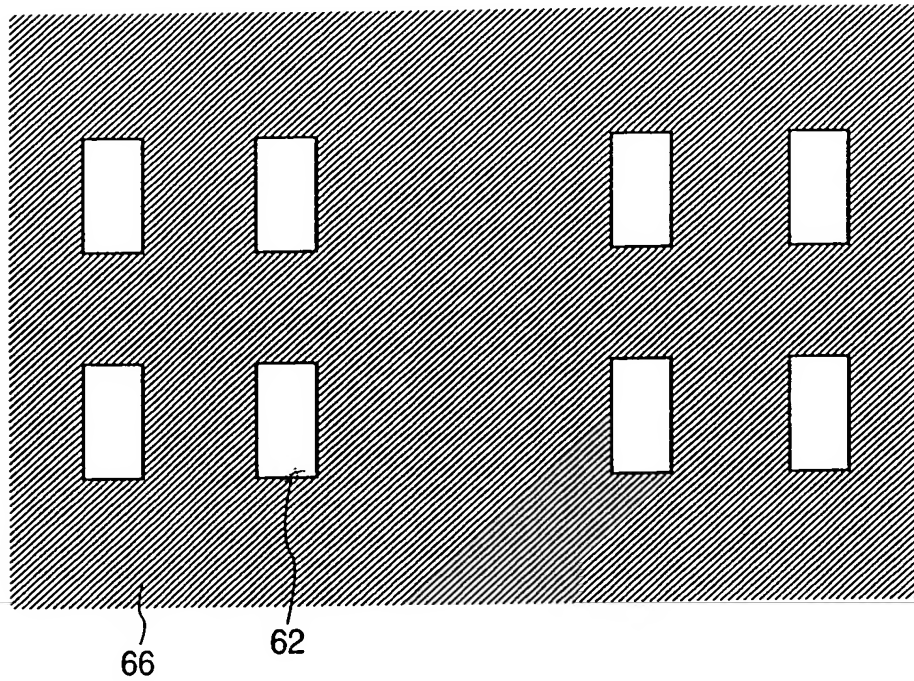


FIG. 43(b)

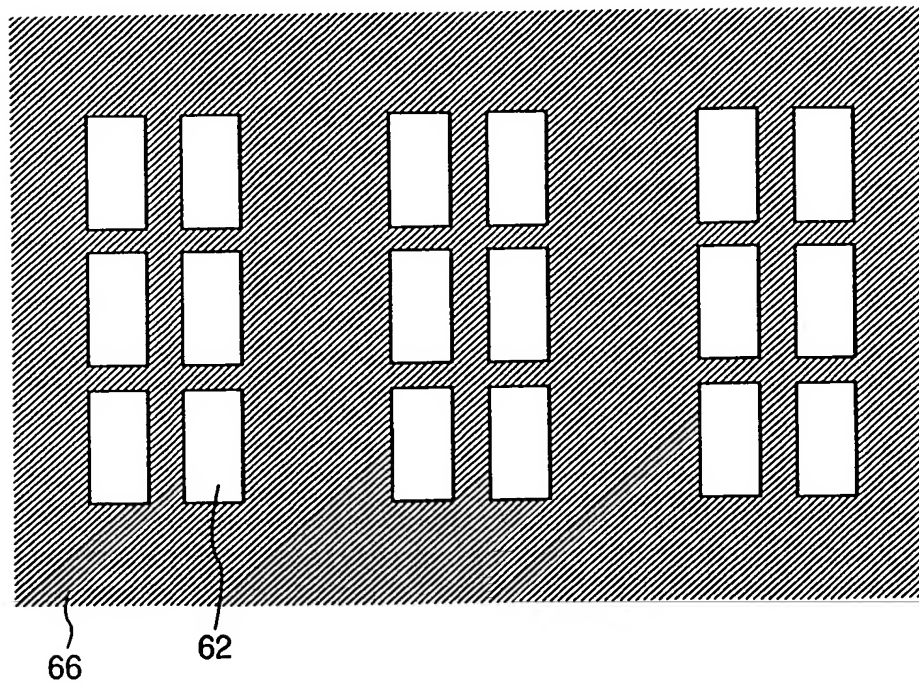


FIG. 44

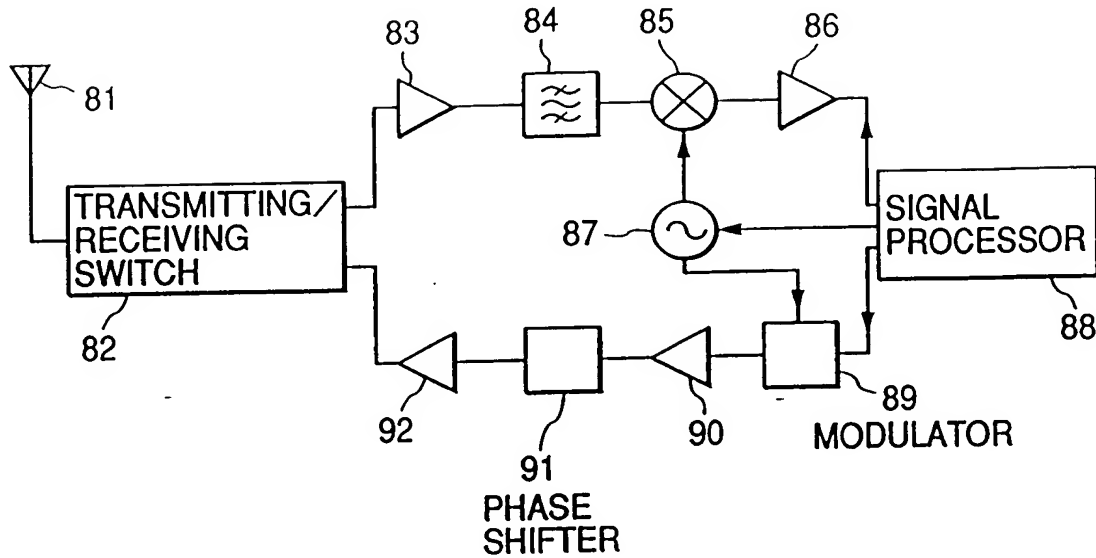


FIG. 45 Prior Art

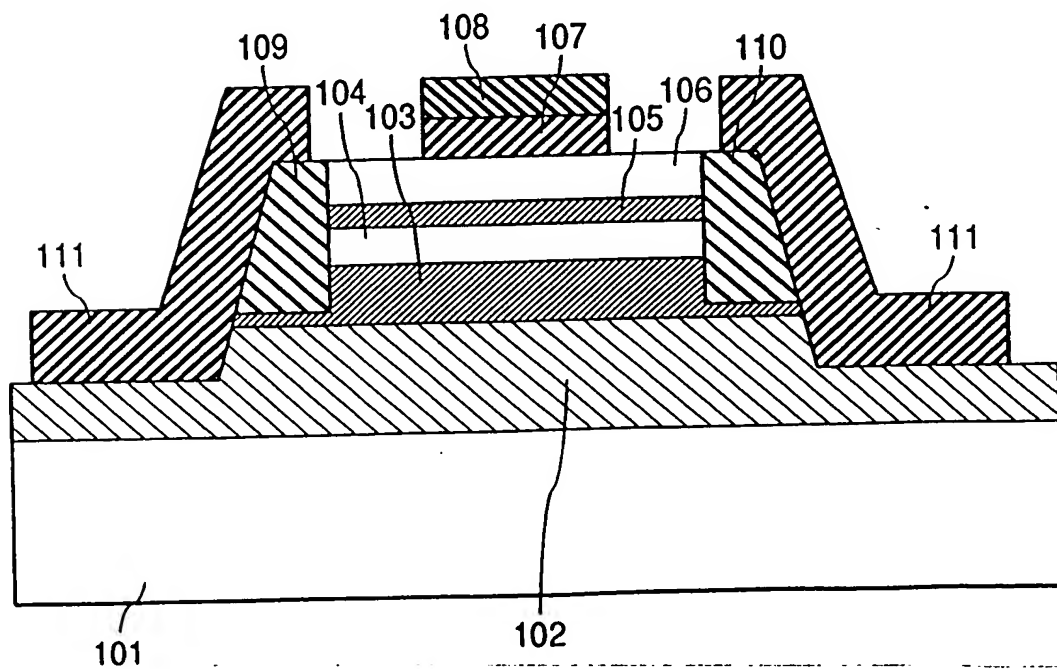


FIG. 46 Prior Art

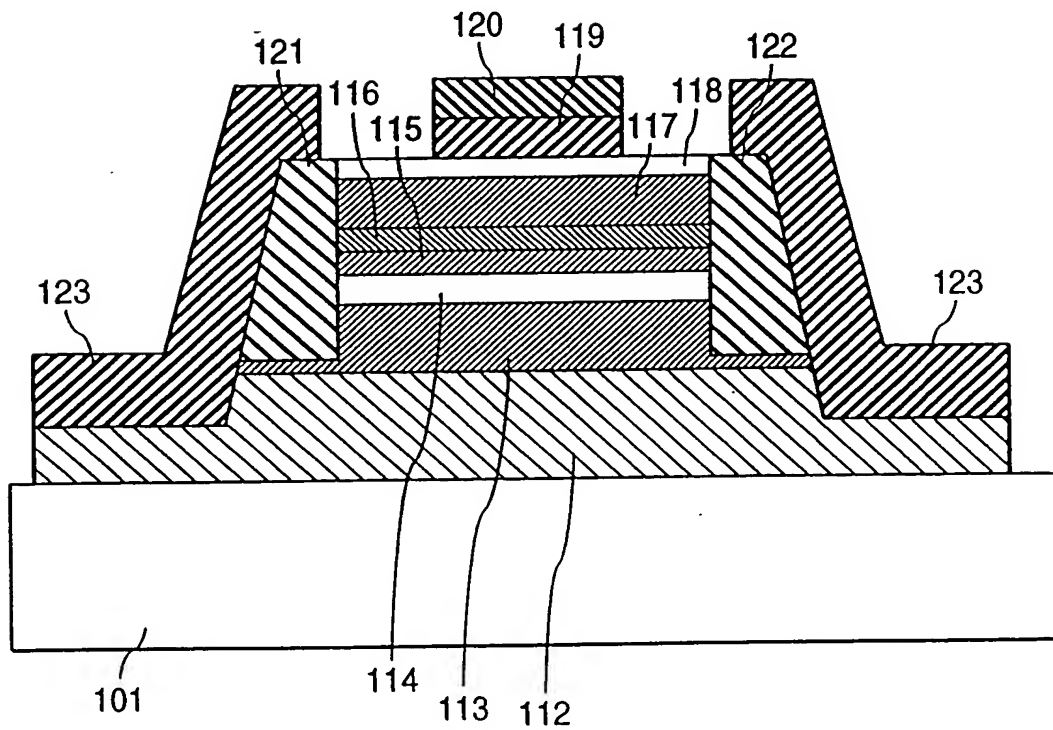


FIG. 47 Prior Art

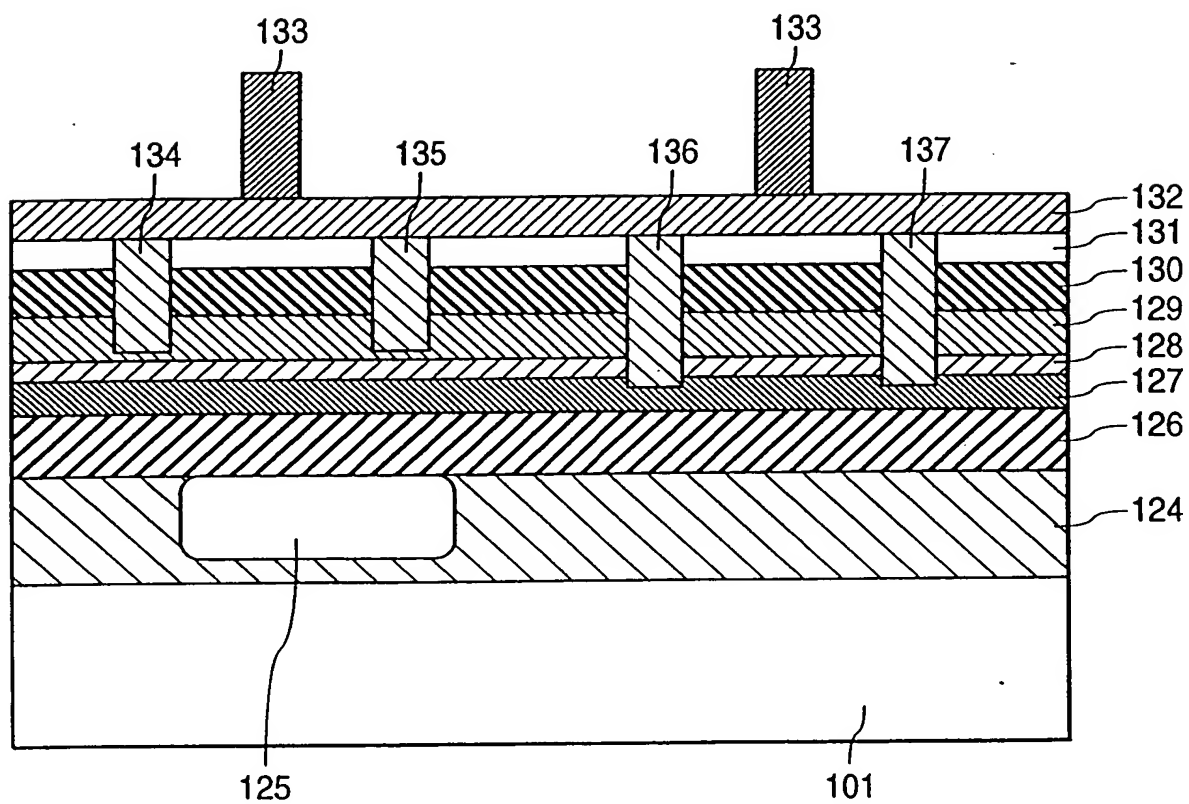


FIG. 48 Prior Art

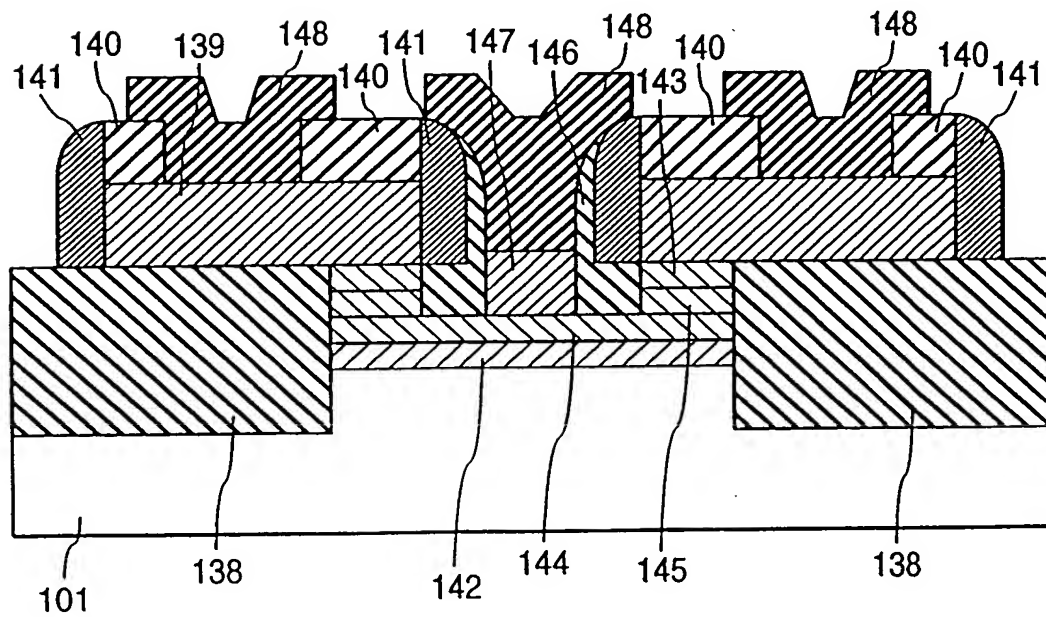


FIG. 49(a) Prior Art

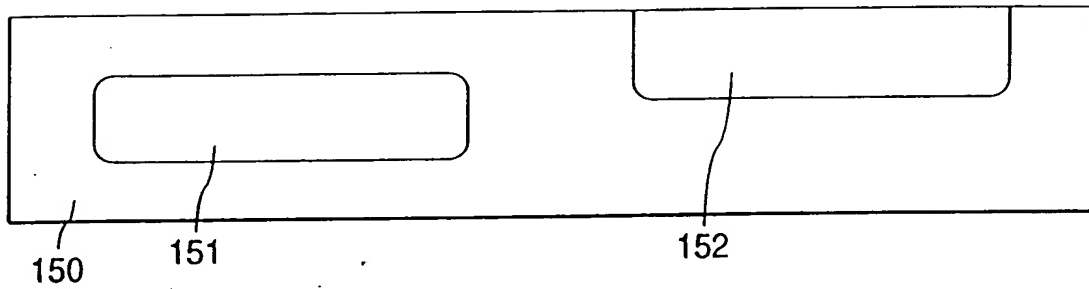


FIG. 49(b) Prior Art

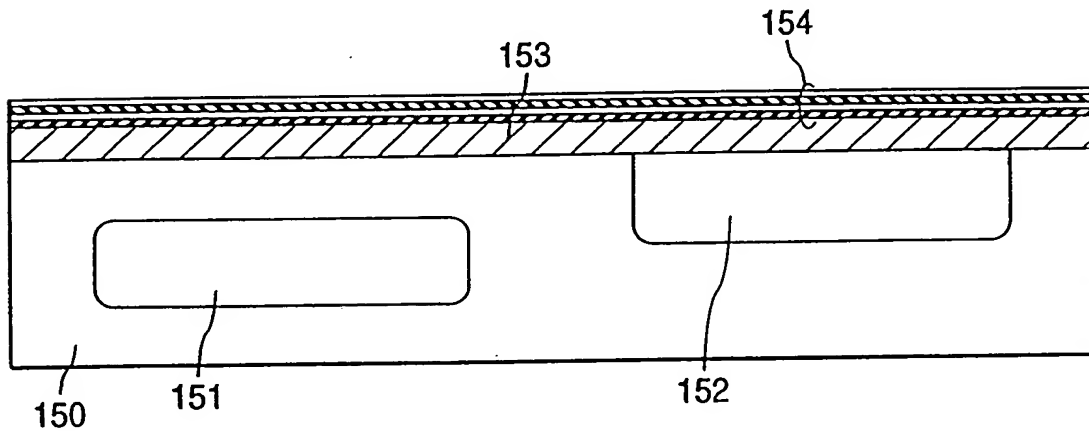


FIG. 49(c) Prior Art

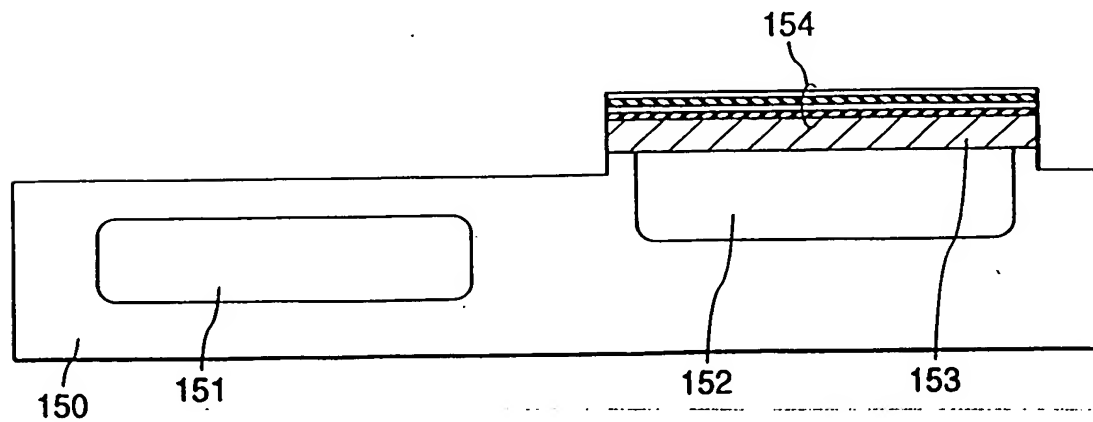


FIG. 50(a) Prior Art

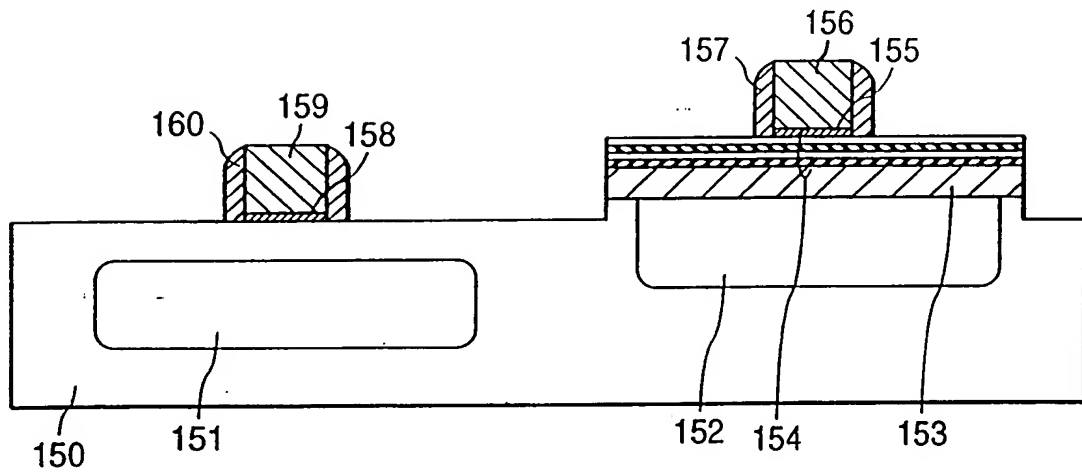


FIG. 50(b) Prior Art

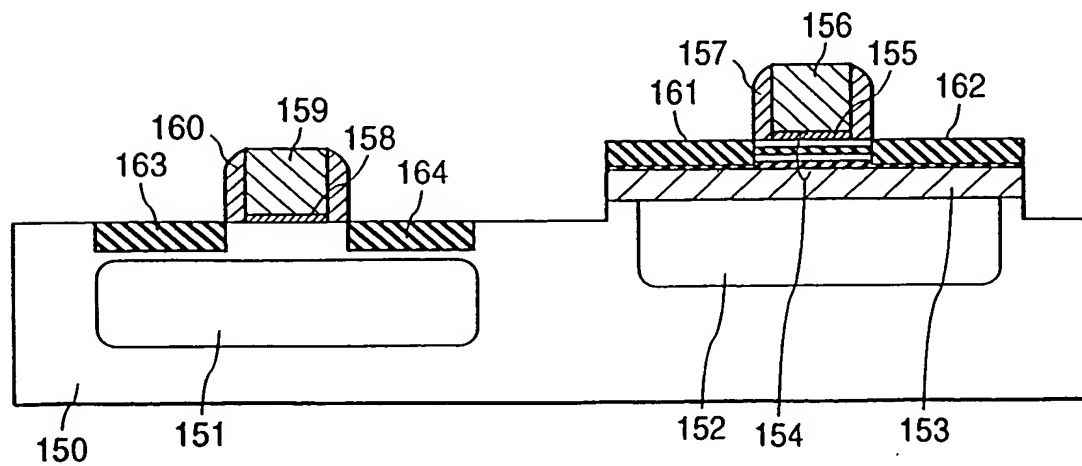


FIG. 51(a) Prior Art

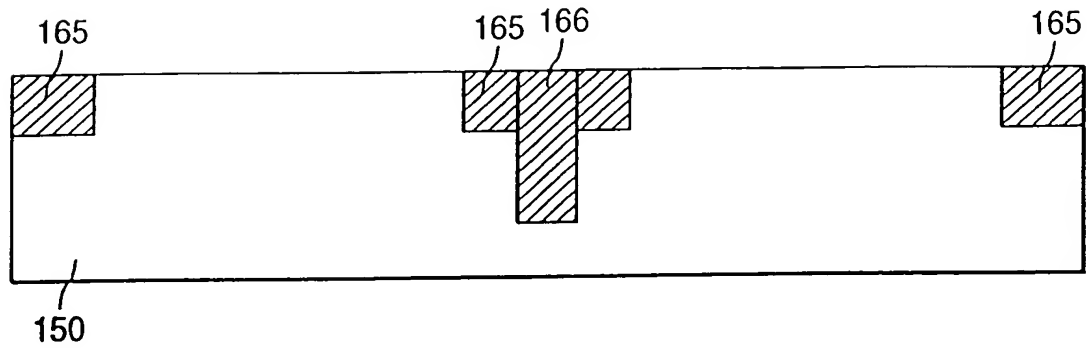


FIG. 51(b) Prior Art

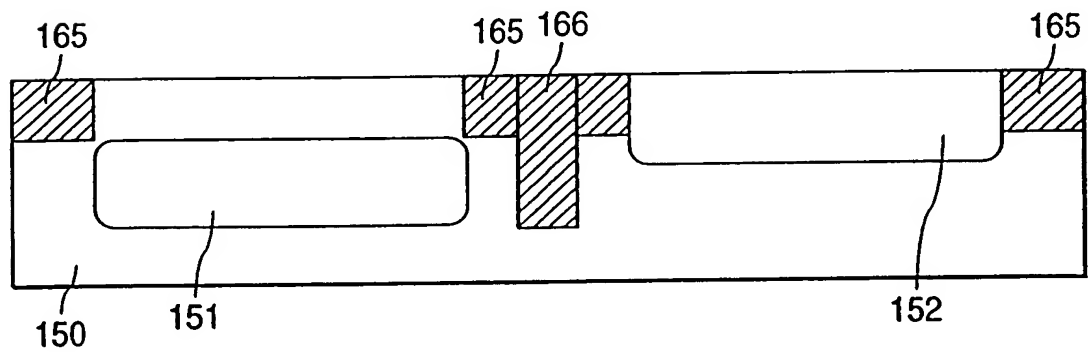


FIG. 51(c) Prior Art

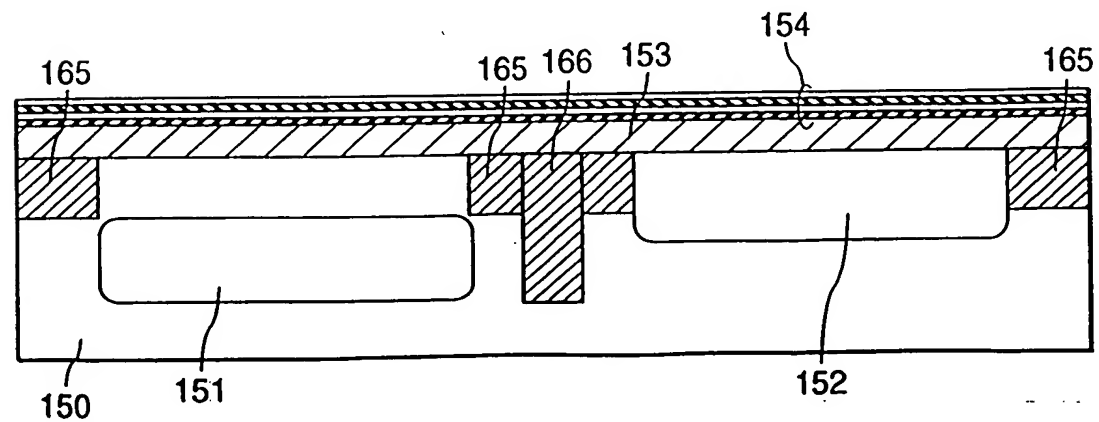


FIG. 52(a) Prior Art

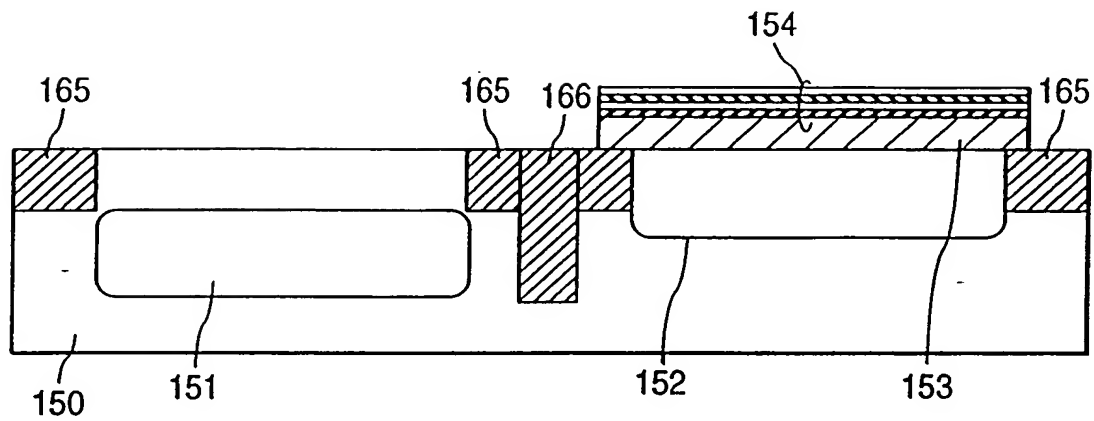


FIG. 52(b) Prior Art

